Attorney Docket No. 211467-00201
12-1128

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant(s):	Tsai, Roger S.
Serial No.:	09/840,500
Filed:	April 23, 2001
Title:	Process Perturbation to Measured Modeled Method for Semiconductor Device Modeling
Group Art Unit:	2123
Examiner:	Stevens, Thomas H..
Confirmation No.:	4458

Applicant's Brief On Appeal

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Table of Contents

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Real Party In Interest

The real party in interest is Northrop Grumman Corporation, by virtue of an Assignment from the inventor Roger Tsai to TRW Inc., recorded on Reel/Frame 011736/0311 and from TRW, Inc., to Northrop Grumman Corporation, recorded on Reel/Frame 013751/0849.

Related Appeals and Interferences

There are no other appeals or interferences known to the Appellant or the Appellant's representative, which are believed to directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status Of Claims

Claims 1-12 are pending. The final rejection of these claims forms the basis for this appeal. In particular, claims 1-4 and 7-12 stand rejected under 35 U.S.C. §102 (b) as being anticipated by

Biswas, Dissertation on "Modeling and Simulation of High Speed Interconnects", 1988 ('the Biswas reference"). Claims 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the Biswas reference in view of VTT Electronics, "Research Activities in Microelectronics", 2000 ("the VTT reference").

Status Of Amendments

All amendments have been entered. The claims as currently amended are attached as an Appendix.

Summary Of Claimed Subject Matter

The present invention relates to a method for modeling semiconductor devices which utilizes a measured-to-modeled microscope as a fundamental analysis basis for constructing a physically-based model by correlating measured-to-modeled performance changes to experimental device changes designed to controllably change physical aspects of the device. The effects of the process perturbation are attributed to changes in measurable internal characteristics of the device. The modeling approach in accordance with the present invention as discussed in connection with Figs. 5-10.

An important aspect of the invention is a measured-to-model microscope (i.e. S-parameter microscope), discussed in connection with Figs. 11-30. The measured –to model microscope utilizes an extraction algorithm, as generally discussed in connection with Figs. 45-50. The measured to model microscope utilizes a filter in exemplary embodiments in order to remove the contribution of device layout parasitics to the modeled electrical characteristics. The filter provides for clearer representations of the internal physical operation for the measured devices. One embodiment of the filter is a Pi-FET filter, discussed in connection with Figs. 26-44.

With thorough process perturbation to measured-modeled PM^2 experimentation, the full range of device performance can be expressed in terms of the microscopes model-basis space, thus forming a single unified compact device technology model, able to accurately model performance changes over a relatively wide range of possible physical and environment changes to the device. The device technology model is able to model internal physical operating mechanisms that dictate the electrical characteristics of the device, such as charge control in FETs or current control in BJTs.

Grounds of Rejection to be Reviewed on Appeal

I. The Examiner rejection of Claims 1-4 and 7-12 as being anticipated under 35 USC §102 (b) in view of the Biswas reference.

II. The Examiner's rejection of Claims 5 and 6 under 35 U.S.C. 103(a) as being unpatentable over the Biswas reference and VTT references.

Argument

I. The Examiner's Rejection of Claims 1-4 and 7-12 as Being Anticipated under 35 USC §102 (b) in View of the Biswas Reference Should Be Reversed.

Claims 1-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by the Biswas reference. In order for there to be anticipation, each and every one of the elements must be found in a single reference. It is respectfully submitted that the claims recite elements clearly not taught or suggested by the Biswas reference. In general, the, the claims teach establishing a physically-representative equivalent model of one or more characteristics of a semiconductor device; varying the physical characteristics; and correcting the model based upon the measured characteristics.

The Biswas reference simply compares commercially available (i.e. "canned") modeling software, namely Layout2FastCap[1], with experimental measurements. The Biswas reference does not disclose testing a semiconductor device and developing a simulation model based on the test data. The Board's attention is respectfully directed to Table 4.2 on page 52 of the Biswas reference, for example.

The table below summarizes the Examiner's contentions that the Biswas reference anticipates the invention, in contrast with the Applicant's arguments. As the table will demonstrate the Biswas reference fails to disclose many elements of the rejected claims and therefore cannot anticipate those claims.

Claim	Examiner's Reference to Biswas	Argument

[1] See abstract of the Biswas reference.

1. A method for modeling one or more predetermined characteristics of a semiconductor device comprising the steps	Page 39, Section 4.1	Section 4.1 relates to measurement techniques
a) fabricating a semiconductor device;	Page 3, lines 11-13	This citation simply comments on recent literature work relating to "chip fabrication."
b) measuring one or more predetermined physical characteristics of said semiconductor device;	Page 6, section 2.4, lines 1-7	
c) testing the semiconductor device; to establish a physically representative equivalent model of said one or more characteristics of said semiconductor device;	Page 42, section 4.4 test chip and , pgs 26, 27, section 3.5.2 and pgs 30, 31 , section 3.5.4	None of the cited sections disclose establishing a physically representative model based upon test data. Indeed, no physical model is established based upon test results, rather, the commercially available FastCap software is used. See Page 26, lines 21 and 22.
d) varying one or more of said predetermined physical characteristics and fabricating a subsequent semiconductor device with said varied dimensions; and	Pages 23, 24 , section 3.5.4	These sections relate to providing "meshed" models of a single inverter in Fig. 3.11 (Two views of the meshed three dimensional view of the CMOS inverter is shown in Figure 3.11." Biswas, page 23). This citation does not disclose fabrication of a

		second semiconductor device, let alone a second device with varied dimensions.
e) testing of the sample to establish a correct said physically representative model.	Page 40, Fig. 4.1	This section simply discloses measurement techniques
2. The method as recited in claim 1, further including the step of measuring the varied dimensions after said subsequent semiconductor is fabricated.	Page 23,24, section 3.4.5	As discussed in connection with element 1d above, the Biswas reference does not disclose fabrication of a second semiconductor device , let alone a second device with varied dimensions.
3. The method as recited in claim 1, wherein a scanning electron microscope (SEM) is used to measure said predetermined dimensions in step (b).	Page 48	The reference to Page 48 does not disclose using the SEM to measure the dimensions of a semiconductor device but rather to "obtain cross section images".
4. The method as recited in claim 1, wherein said testing in step (c) includes taking S-parameter measurements of said semiconductor device.	Page 51	
7. The method as recited in claim 1, wherein said varied dimensions are measured by	Page 48	As mentioned in connection with Claim 3, the SEM is used for a purpose other than the

way of an SEM.		purpose recited in this element.
8. The method as recited in claim 1, wherein said corrected physically representative model is corrected based upon S-parameter measurements.	Page 48	As mentioned above, the Biswas reference simply compares simulated results from commercially available software with actual test results. The Biswas reference does not disclose or suggest modifying the analytical model based upon the test results.
9. A process for making a semiconductor device comprising the steps of:		See claim 1
a) fabricating a semiconductor device;	Page 3, lines 11-13	See comments in re element 1a above.
b) measuring one or more predetermined physical characteristics defining measured characteristics of said semiconductor device;	Pg. 6, section 2.4, lines 1-7	
c) testing said semiconductor device to establish a physically representative model;	Pg. 42, section 4.4 test chip	See comments in re element 1c above.
d) fabricating a subsequent semiconductor device in which said one or more measured characteristics	Pg. 3, lines 11-13	See comments in re element 1d above.

are varied; defining varied characteristics.		
e) measuring said varied characteristics; and	Pg. 36	The Biswas reference does not disclose a second device with varied characteristics and measurement of those varied characteristics to develop a revised analytical model.
f) testing said semiconductor device to establish a revised physically representative model of said semiconductor device.	Pg. 40, Fig. 4.1	See comments in re element 1e above.
10. The process as recited in claim 9, further including step (g) repeating steps (d) through (f) one or more times.	Pg. 3, lines 11-13	See comments for Claim 9 above.
11. The process as recited in claim 9, wherein said physically representative model in steps (c) and (b) is based on predetermined S-parameter measurements.	Pg. 6, line 7.	The Biswas reference does not disclose developing a second semiconductor device based upon S- parameter measurements.
12. The process as recited in claim 9, wherein steps (b) and (c) include measurement by way of a scanning electron microscope.	Page 48	Although the Biswas discloses the use of a SEM, it is used for a different purpose than the recited in steps (b) and (c).

Based on the above, it is respectfully submitted the Biswas reference fails to disclose many of the elements of the Claims 1-4 and 7-12. Accordingly, the Board is respectfully requested to reverse the Examiner on this issue.

II The Examiner's rejection of Claims 5 and 6 under 35 U.S.C. § 103(a) as being Unpatentable over the Biswas Reference Should Be Reversed.

Claims 5 and 6 were rejected under Biswas in further review of the VTT reference. The Biswas reference was discussed above. It is respectfully submitted that the VTT reference likewise does not teach creating a simulation model building a semiconductor device and using test measurements from the semiconductor device to modify the simulation model. Moreover, it is respectfully submitted that the Examiner has failed to set forth a *prima facie* case of obviousness as required by MPEP §2143.

More particularly, § 2143 of the MPEP requires:

> *"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference, or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claim combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure."*

It is respectfully submitted that the Examiner's rejection fails to meet all three criteria set forth in § 2143 of the MPEP. First, the Examiner has failed to show any suggestion or motivation to combine the references in the manner stated. The Examiner simply opines the combination would be obvious. Second, without using the claims as a blueprint, the Examiner has failed to show a reasonable expectation or any expectation for that matter of the of the success of the proposed combination . Finally, as discussed above, the Biswas reference fails to disclose all of the elements of the claims. The missing elements are likewise not disclosed in the VTT reference.

For these reasons and the reasons submitted above, the Board is respectfully requested to reverse the rejection of claims 5 and 6.

Conclusion

The Board is respectfully requested to reverse the rejections of all claims by the Examiner.

Respectfully Submitted,

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Appendix A
Claims On Appeal

1. A method for modeling one or more predetermined characteristics of a semiconductor device comprising the steps:

a) fabricating a semiconductor device;

b) measuring one or more predetermined physical characteristics of said semiconductor device;

c) testing the semiconductor device; to establish a physically representative equivalent model of said one or more characteristics of said semiconductor device;

d) varying one or more of said predetermined physical characteristics and fabricating a subsequent semiconductor device with said varied dimensions; and

e) testing of the sample to establish a correct said physically representative model.

2. The method as recited in claim 1, further including the step of measuring the varied dimensions after said subsequent semiconductor is fabricated.

3. The method as recited in claim 1, wherein a scanning electron microscope (SEM) is used to measure said predetermined dimensions in step (b).

4. The method as recited in claim 1, wherein said testing in step (c) includes taking S-parameter measurements of said semiconductor device.

5. The method as recited in claim 1, wherein said one or more predetermined characteristics include device scaling; bias dependence; temperature dependence; lay out dependence and process dependence.

6. The method as recited in claim 1, wherein said one or more predetermined physical characteristics include the physical dimensions of the source access regions of said semiconductor device.

7. The method as recited in claim 1, wherein said varied dimensions are measured by way of an SEM.

8. The method as recited in claim 1, wherein said corrected physically representative model is corrected based upon S-parameter measurements.

9. A process for making a semiconductor device comprising the steps of:

a) fabricating a semiconductor device;

b) measuring one or more predetermined physical characteristics defining measured characteristics of said semiconductor device;

c) testing said semiconductor device to establish a physically representative model;

d) fabricating a subsequent semiconductor device in which said one or more measured characteristics are varied; defining varied characteristics.

e) measuring said varied characteristics; and

f) testing said semiconductor device to establish a revised physically representative model of said semiconductor device.

10. The process as recited in claim 9, further including step (g) repeating steps (d) through (f) one or more times.

11. The process as recited in claim 9, wherein said physically representative model in steps (c) and (b) is based on predetermined S-parameter measurements.

12. The process as recited in claim 9, wherein steps (b) and (c) include measurement by way of a scanning electron microscope.

Appendix B
Evidence Appendix

None

APPENDIX C
RELATED PROCEEDINGS APPENDIX

None